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(54) **V-MOS field effect semiconductor device**

(57) A power, V-grooved MOSFET semiconductor device has V-grooves 31,32 extending in two orthogonal dimensions, thereby forming a semi-continuous mesh grid configuration which maximizes the periphery of the MOSFET channels for a given area of silicon, thus providing higher output current and lower "on resistance" for a given area than a conventional, inter-digitated V-MOS power transistor having V-grooves running in only one dimension. A plurality of devices may be formed in one wafer.
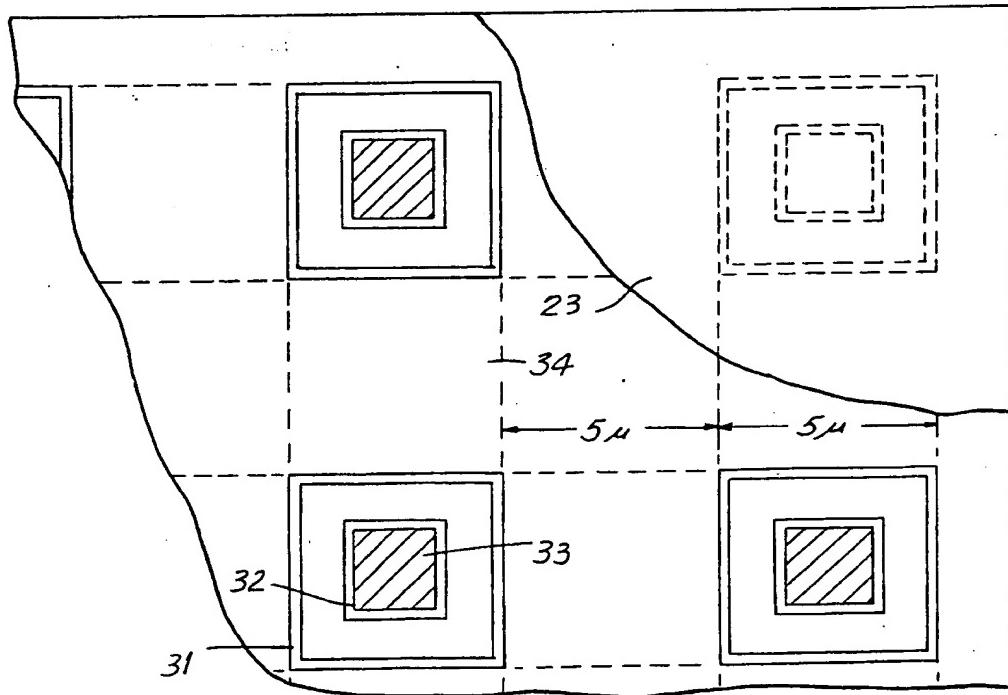
FIG. 10

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FIG. 1

FIG. 2

FIG. 3

FIG. 4

FIG. 5

FIG.6

FIG.7

FIG.8

FIG.9

FIG. 10

23
34
5µ   5µ
33
32
31

FIG. 11

SOURCE   SOURCE   SOURCE

CELL AREA 47
2½µ   2½µ
41   42
3µ
SOURCE   SOURCE   SOURCE
46

1µ
1µ   43   44
SOURCE   SOURCE   SOURCE

5µ   5µ
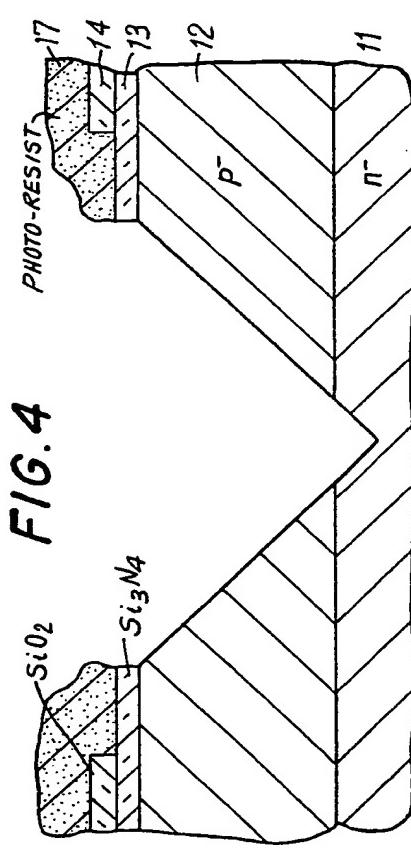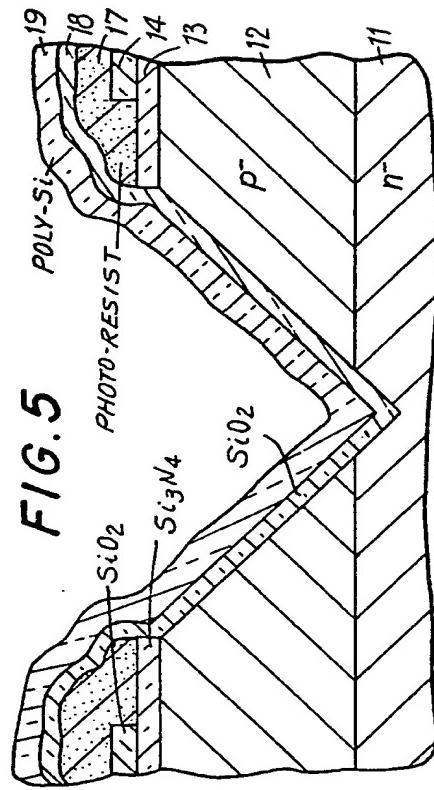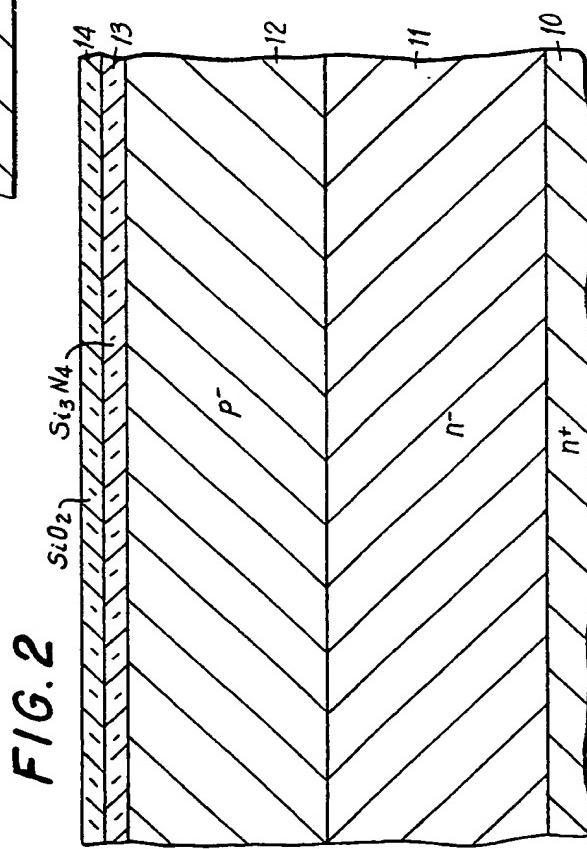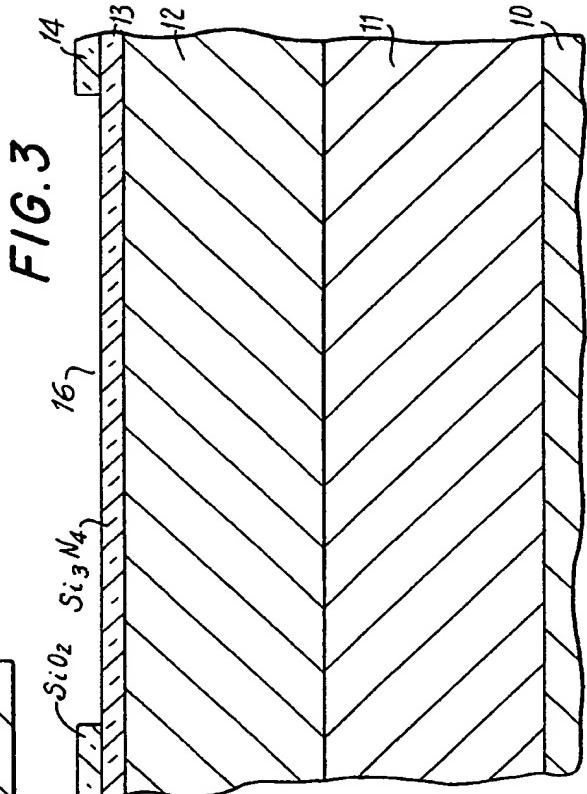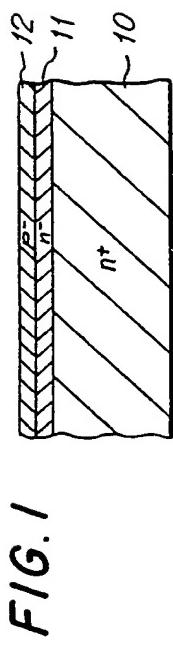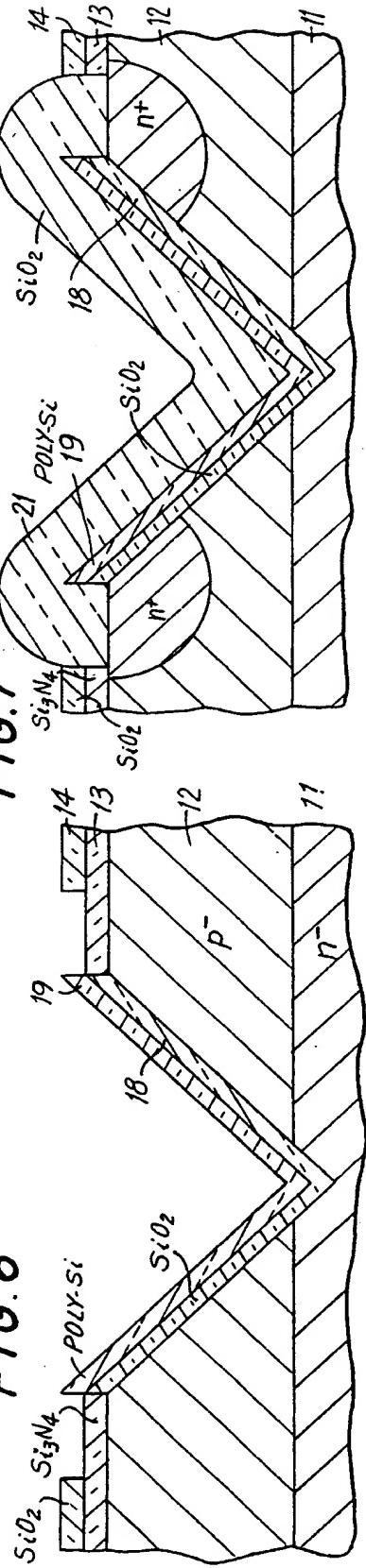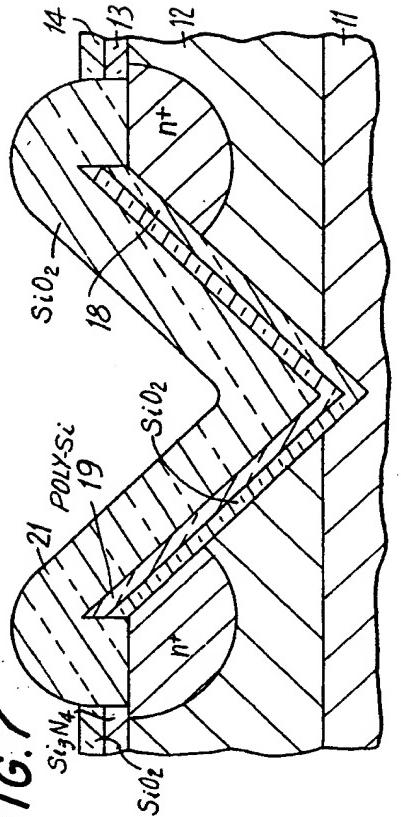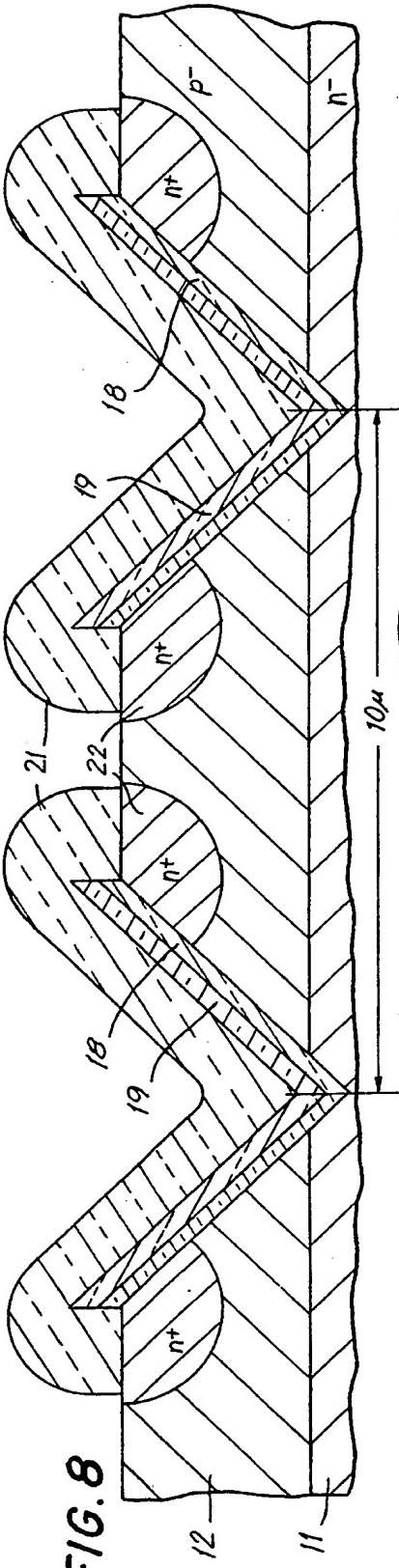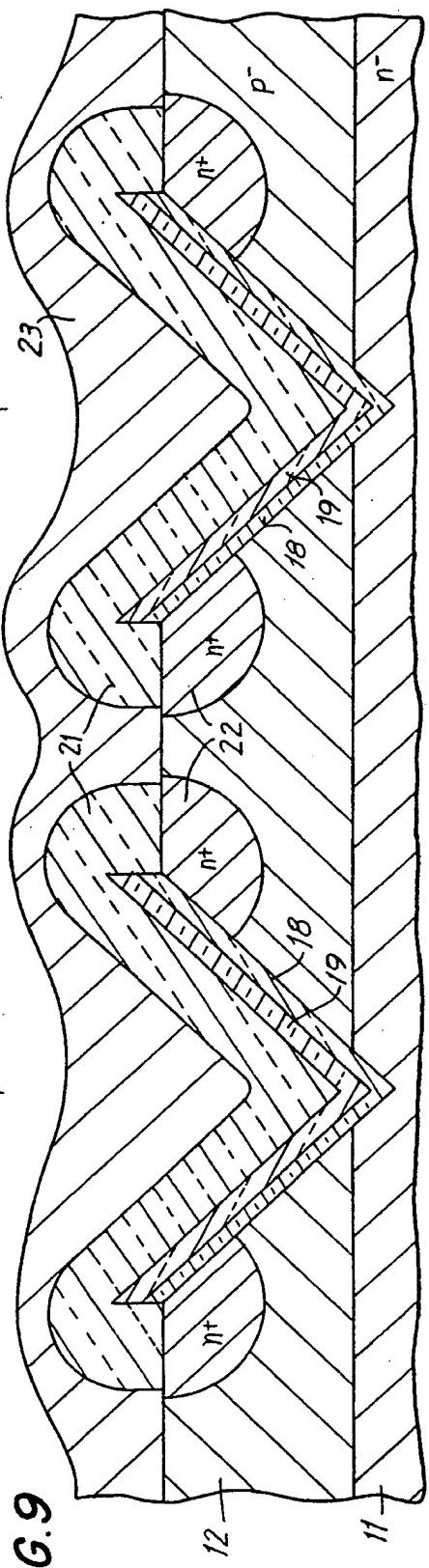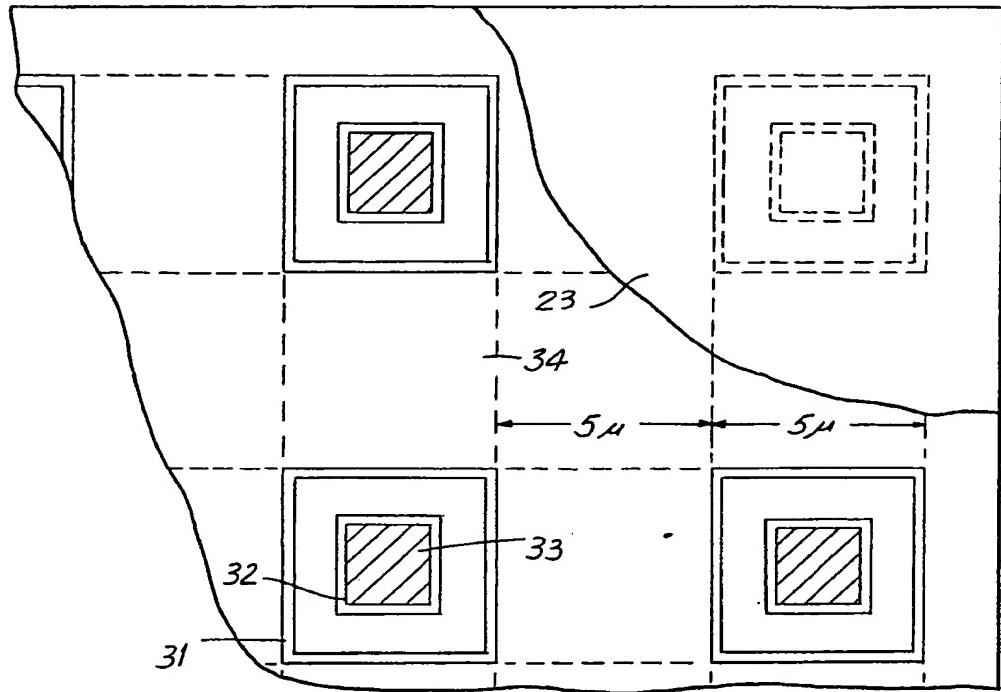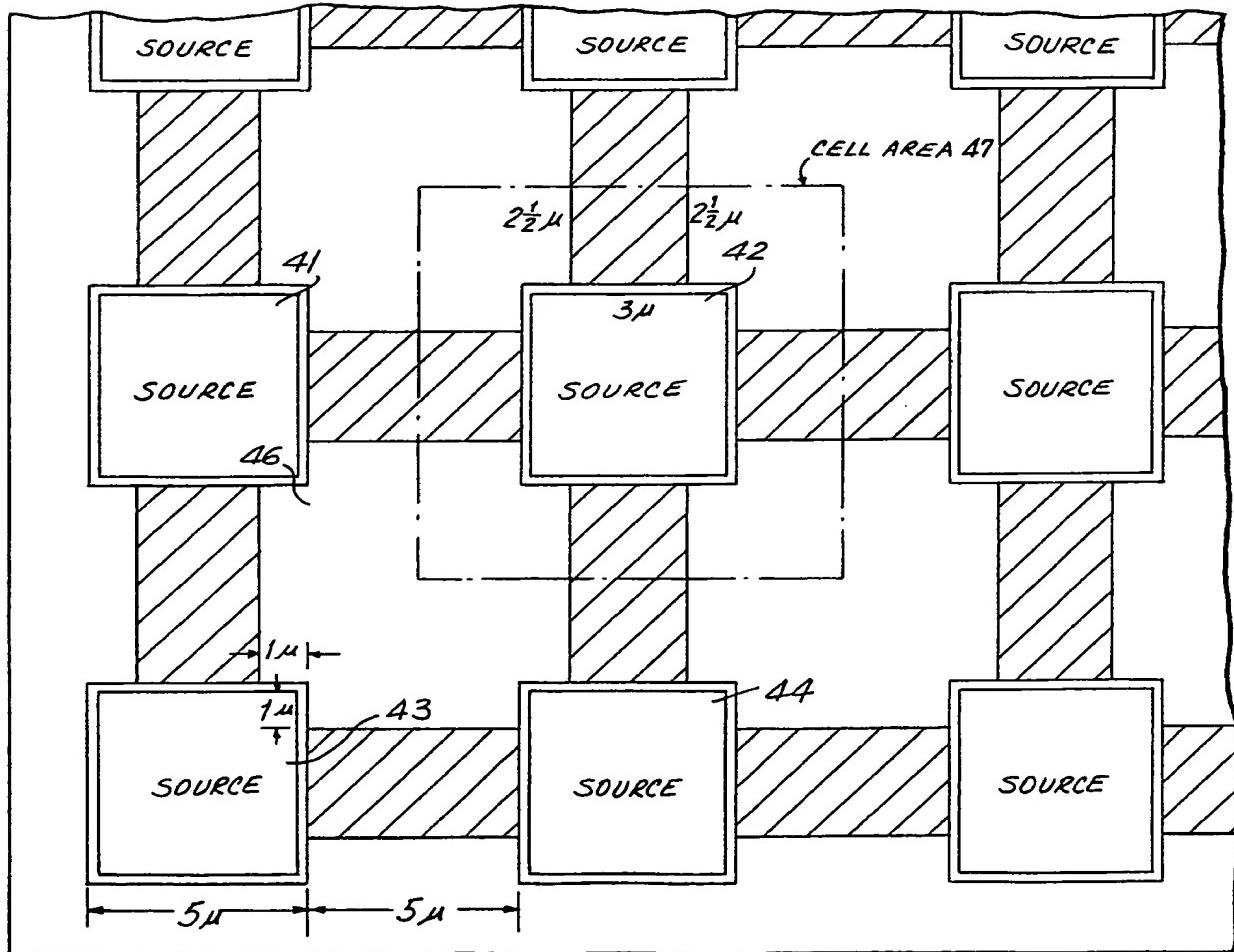
FIG.12
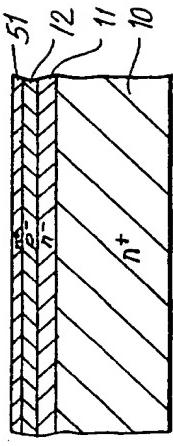
FIG.13
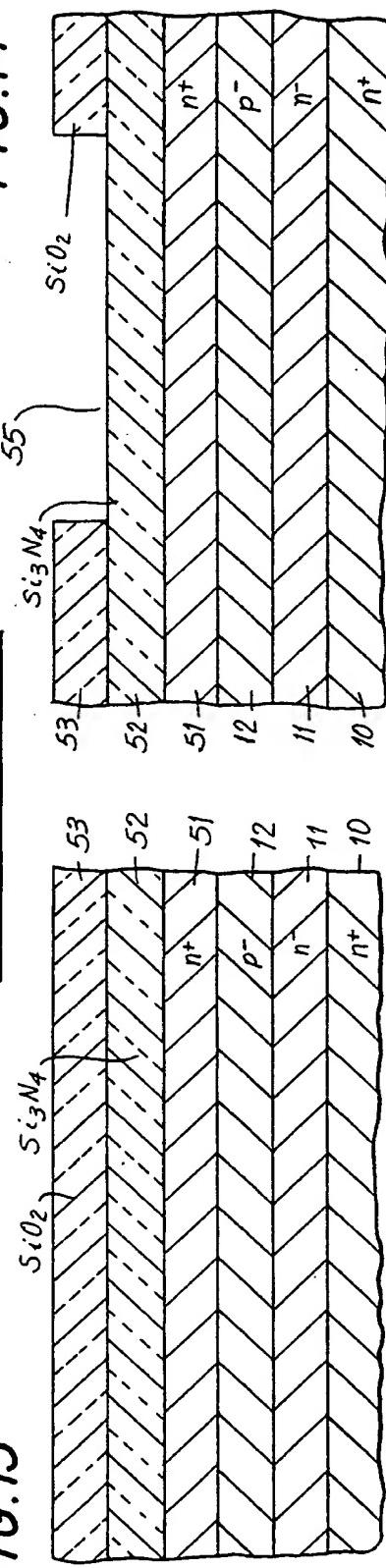
FIG.14
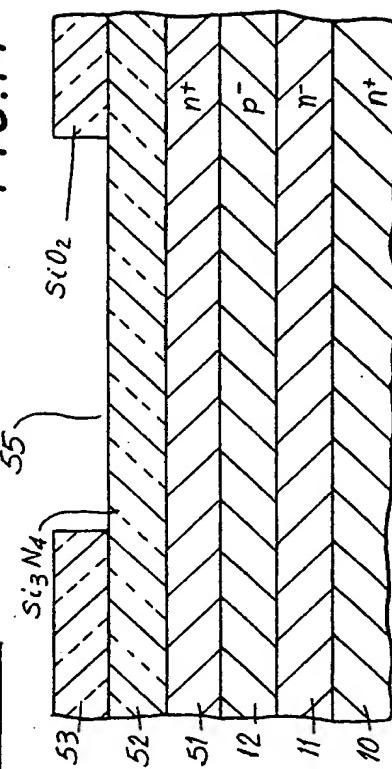
FIG.15
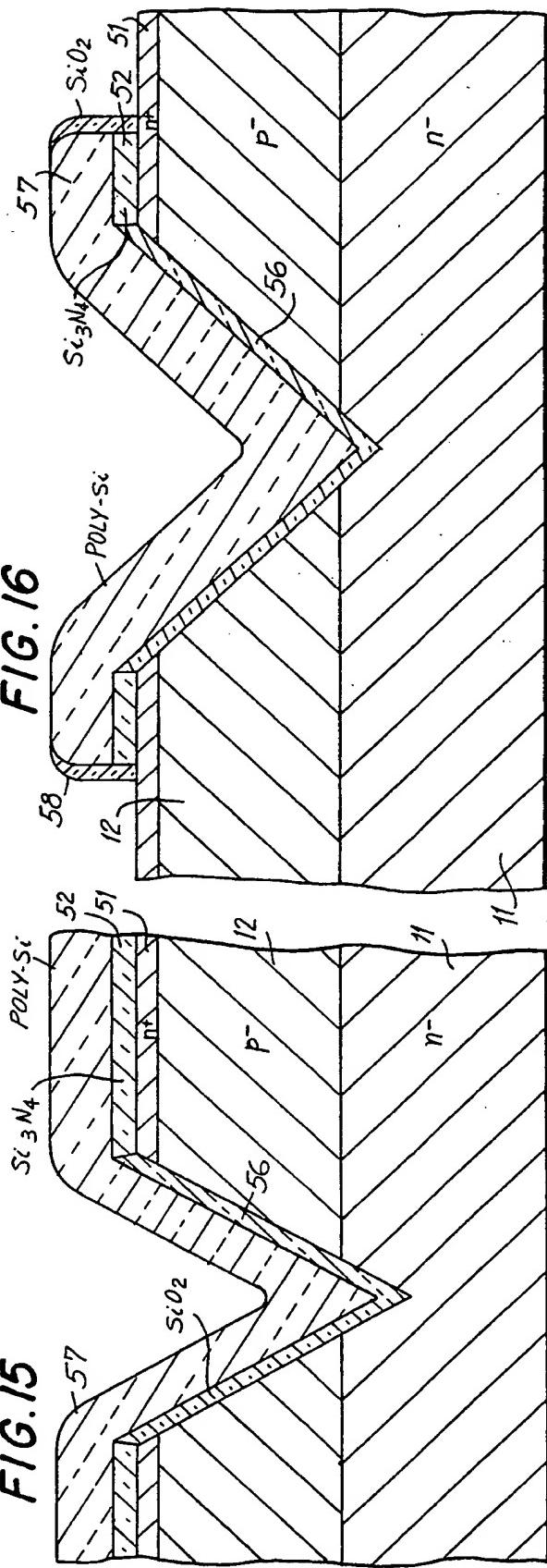
FIG.16
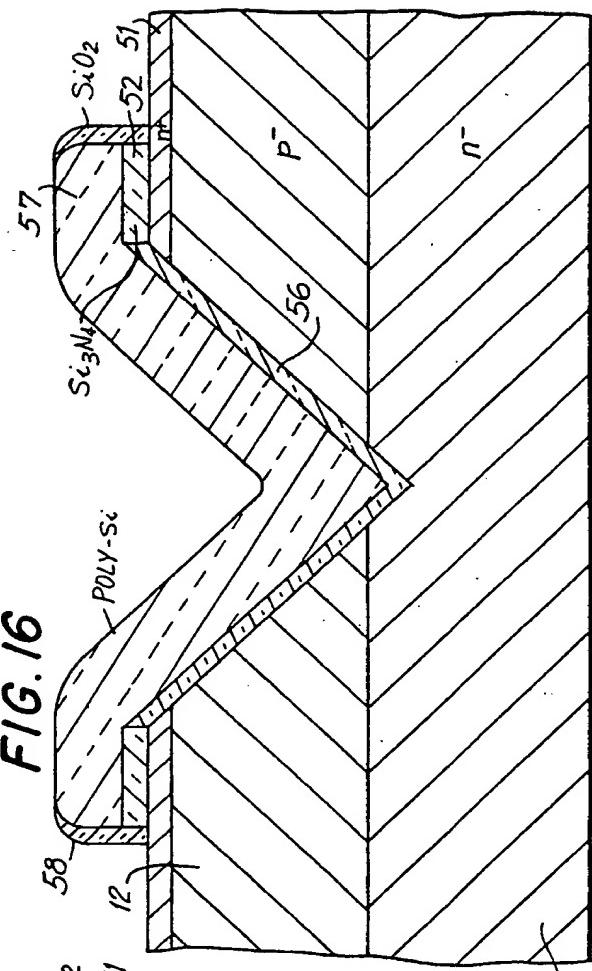
SPECIFICATION

V-MOS field effect semiconductor device

5 Broadly speaking, this invention relates to semiconductor devices. More particularly, in a preferred embodiment, this invention relates to a V-groove, MOSFET, power, semi-conductor device and methods for manufacturing the same.

10 Semi-conductor devices intended for high-power applications may be manufactured in any of several configurations including bipolar and MOSFET; however, MOSFET devices offer several advantages over bipolar devices. Among these are (1) a greater

15 safe operating area which results from the fact that MOSFET devices have an inherent negative temperature co-efficient of current versus temperature; (2) MOSFET devices may be controlled by a low gate-drive current and may therefore be directly driven by

20 the output of MOS LSI output stages; (3) MOSFET devices have an extremely fast turn-off since no minority carrier storage effects are present; and (4) MOSFET devices are free from secondary breakdown because no current hogging is present.

25 Of course, MOSFET devices themselves can be manufactured in a variety of configurations. However, recently considerable interest has been expressed in V-grooved MOSFET, sometimes referred to as V-MOS devices, which exhibit several advantages

30 over MOSFET devices of conventional design. See, for example, the article entitled "A High Power Mosfet With Vertical Drain Electrode and Meshed Gate Structure" by Yoshida, Kubo and Ochi, *IEEE Journal of Solid State Circuits,* Volume SC-11, Num-

35 ber 4, August, 1976, and "V-MOS, A Breakthrough in Power MOSFET Technology" by Shaeffer, Siliconix, Inc., Application Note AN76-3, May, 1976.

Unfortunately, prior art V-grooved MOSFET devices, although representing a significant advance

40 over conventional devices, have nevertheless not gained the acceptance that had been hoped. This is due, in part, to the higher cost of V-MOS which is caused, in turn, by the increased complexity of manufacture. Particularly troublesome are the large

45 number of critical photomask operations that must be performed to manufacture a V-grooved MOSFET device.

The object of this invention, therefore, is to provide a V-groove MOSFET architecture that over-

50 comes all of the deficiencies noted above with respect to conventional V-groove MOSFET devices.

In fulfillment of the above and other objectives, the instant invention comprises a V-MOS, field-effect, semiconductor device, having gate, source and drain

55 electrodes. The device comprises a planar, doped silicon substrate; a first, doped, silicon layer epitaxially grown on the silicon substrate; a second, doped, silicon layer epitaxially grown on the first silicon layer; at least two, spaced-apart, parallel, first

60 V-grooves extending partially thru the first and completely thru the second layers but not into the substrate; at least two, spaced-apart, parallel, second V-grooves extending through the first and second layers into the substrate, the first and second

65 V-grooves having doped poly-silicon on the walls

thereof, being orthogonally oriented with respect to one another and and defining by their intersection at least one generally rectangular, isolated, electrically floating region of the second doped layer which acts

70 as the substrate electrode of the device, the remaining non-isolated regions of the second layer acting as the gate electrode of the device, the substrate acting as the drain electrode.

The invention and its mode of operation will be

75 more fully understood from the following detailed description when taken with the appended drawings.

Figure 1 is a cross-sectional view of a silicon substrate for use with a device according to the

80 invention;

Figure 2 is a cross-sectional view of the substrate shown in Figure 1 after additional processing steps have taken place thereon;

Figure 3 is a cross-sectional view of the substrate

85 shown in Figure 2 after a first photo-lithographic processing step has been effected;

Figure 4 is a cross-section of the substrate shown in Figure 3 after a V-groove has been opened therein;

90 *Figure 5* is a cross-sectional view of the substrate shown in Figure 4 after the V-groove has been coated with a layer of silicon dioxide and poly-silicon;

Figure 6 is a cross-sectional view of the substrate

95 shown in Figure 5 after additional processing steps have been effected;

Figure 7 is a cross-sectional view of the substrate shown in Figure 6 after an additional layer of silicon dioxide has been grown over the V-grooves;

100 *Figure 8* is a cross-sectional view showin two adjacent V-grooves and a common substrate;

Figure 9 is a cross-sectional view of the substrate shown in Figure 8 after metalization has been grown over the entire upper surface of the device;

105 *Figure 10* is a planar view of a portion of a semiconductor wafer showing a plurality of devices according to the invention;

Figure 11 is a plan view of an alternate embodiment of the invention in which additional source

110 material is formed adjacent to each of the devices to reduce etching undercutting;

Figure 12 is a cross-sectional view of a substrate used in manufacture of an alternative embodiment of the invention;

115 *Figure 13* is a cross-sectional view of the substrate shown in Figure 12 after additional processing steps have been effected;

Figure 14 is a cross-sectional view of the substrate shown in Figure 13 after a first photo-lithographic

120 processing step has taken place;

Figure 15 is a cross-sectional view of the substrate shown in Figure 14 after a V-groove has been opened therein; and

Figure 16 is a cross-sectional view of the substrate

125 shown in Figure 15 after the V-groove has been coated with a layer of doped poly-silicon.

The first illustrative embodiment of the invention to be discussed comprises a V-grooved power MOSFET having V-grooves that extend in two ortho-

130 gonal dimensions thereby to form a semi-

continuous grid configuration. Such a configuration
maximizes the periphery of the MOSFET channel for
any given area of silicon and, therefore, yields higher
output current and lower "on resistance" for a given
5 area of silicon than a conventional, interdigitated
V-MOS power transistor having V-grooves extend-
ing in only one dimension. As will be explained, a
further advantage of this grid-like gate structure is
that, although the contact to the polysilicon in the
10 device is made in a bonding area positioned away
from the active gate grooves, the series resistance
γS of the gate is drastically reduced, due to the
semicontinuous nature of its structure. This, in turn,
will give an improved frequency response since the
15 gate.product, i.e., the product of γS times Cg, the
gate capacitance, is correspondingly reduced.
   As shown in Figure 1, the first step in the
manufacture of a device according to the invention is
to grow a relatively lightly doped n− epitaxial silicon
20 layer 11 upon a heavily doped n+ silicon substrate
10. A second epitaxial layer 12 of p-type material is
then grown on top of the first epitaxial layer 11, as
shown. The thickness and resistivity of the first layer
11 is, of course, dependent upon the breakdown
25 voltage BVDSS of the device under fabrication. In
like fashion, the thickness and resistivity of the
second epitaxial layer 12 depends upon the
threshold voltage and punchthrough voltage from
drain to source of the device being fabricated. The
30 thickness of the second epitaxial layer is also
determined by the surface V-groove gate openings
with a minimum thickness equal to approximately
$0.7 \times Xg$ (opening). For a device having a breakdown
voltage of from 40 to 60 volts, say, epitaxial layer 11
35 will have a thickness of 4 microns and a resistivity of
0.8 ohm-centimeters. The thickness and resistivity of
epitaxial layer 12 will be 3 microns and .3 to .5
ohm-centimeters, respectively. Obviously, for higher
breakdown voltages the resistivity of the n− eipta-
40 xial layer 11 will increase. For example, for a 450 volt
breakdown device, this layer would have a thickness
in the order of 25 microns with a resistivity of 12.5
ohm-centimeters.
   To achieve still higher breakdown voltages, it has
45 been discovered that the surface electric field of the
device may be contoured by the use of floating p−
rings. According to the invention, these rings are
obtained by continuing the V-grooving along the
outside periphery of the active area to form isolated
50 p− regions which are left electrically floating and
which serve to spread the depletion layer laterally so
that the electric field created by the drain-to-source
potential can be reduced. The number of floating p−
rings, and the center-to-center spacing required to
55 raise the breakdown voltage to the theoretical limit
for a plane junction, is determined empirically.
   Where the circuit applications are such as to
require reverse blocking in addition to the normal
forward blocking obtained from any MOSFET de-
60 vice, a p+ substrate may be substituted for the n+
substrate 10 shown in Figure 1. If this is done, and
the same or similar double eiptaxial layers are
grown on the substrate, the drain-to-source voltage
can go negative (for an n channel structure) and the
65 n− to p+ substrate junction will then block voltages

up to the breakdown voltage of that junction. In this
manner, a MOSFET device according to the inven-
tion will function similarly to a thyristor device.
   In order to achieve maximum power density, the
70 source and gate V-groove cells are advantageously
positioned as close as possible to one another. This
will have the additional advantage of producing the
lowest possible cost per device since chip size is
reduced for a given output current or "on resist-
75 ance" level. In addition, it is well-known that device
yield depends inversely upon the number of photo-
lithographic steps required to produce a device.
Hence, reducing the number of steps will, of necessi-
ty, increase yield and further reduce chip cost.
80   Turning now to Figure 2, the manufacturer of a
V-groove device according to the invention begins
with an n+ or p+ silicon substrate 10 of 100 crystal
orientation having a first epitaxially grown n− layer
11 and a second epitaxial p− layer 12 thereon. Next,
85 a layer of silicon nitride 13 is deposited on the p−
epitaxial layer 12 to a depth of approximately 2,000 Å
units. Next, a layer of silicon dioxide 14 is deposited
over the layer of silicon nitride using either a high or
low temperature deposition process, again to a
90 depth of approximately 2,000 Å. Next, as shown in
Figure 3, by the use of any of several known
photo-lithographic techniques, the regions 16 which
are to form the source and gate grooves are opened
up, e.g., by etching a patterned photo-resist over-
95 layed on the silicon dioxide layer 14. By the use of an
appropriate etchant, for example, a standard buf-
fered HF etch, the silicon dioxide only is etched away
with the etching process terminating automatically
when the etchant reaches the Si_3N_4 silicon nitride
100 layer 13.
   Next, as shown in Figure 4, a second photo-
lithographic process is used to open up the V-groove
areas only. Incidentally, this is the only critical
alignment step in the manufacture of this device. As
105 shown in Figure 4, a layer of photoresist 17 is
overlaid on the patterned silicon dioxide mask 14
which, after exposure and development, is then
etched by the use of any suitable etching process,
such as a hot phosphoric acid etch or a plasma etch,
110 to eat through silicon nitride layer 13 thereby
forming the desired V-groove opening in the p−
material 12, which groove extends at its lower end
down into the n− material 11.
   As shown in Figure 5, without removing photore-
115 sist layer 17, the next step in the process is to deposit
a layer 18 of silicon dioxide over the entire V-groove
region using some suitable low temperature plasma
deposition process. Advantageously, the plasma
deposition process takes place at a temperature of
120 approximately 25°C, although temperatures as high
as 250°C may be tolerated. The depth of the silicon
dioxide layer is not critical but should be in the order
of 1500 Å. Next, a layer 19 of pure poly-silicon is
sputtered over the entire surface to a depth of 10,000
125 Å. Now, as is well-known, the deposited silicon and
the sputtered polysilicon will not adhere well to
photoresist 17. Thus, as shown in Figure 6, photore-
sist 17 can easily be stripped chemically, or by the
use of some plasma etching process, which will lift
130 off the SiO_2 and the poly-silicon everywhere except

in the groove areas.

Next, the density of the deposited films is in-
creased, for example, by exposing the films to
elevated temperatures in the range of 900°C to
5 1100°C in a nitrogen atmosphere. Then, the entire
wafer is etched, for example, by exposing the wafer
to some suitable etch that is capable of dissolving
silicon nitride, for example, a plasma etch or some
suitable chemical etch, to expose the p— silicon
10 region adjacent to the groove areas. These areas are
identified by reference numeral 22 in Figure 7. Next,
the entire slice is exposed to an n+ dopant, such as
phophorous or arsenic, e.g., by diffusion. The layers
of SiO$_2$ and Si$_3$N$_4$ 14 and 13, respectively, will mask
15 the diffusants from the p— layer 12 except, of course,
in regions 22 adjacent to the groove areas which,
thus, become doped to n+ material, as is the
poly-silicon layer 19 in the groove. Next, the n+
diffusants are driven into the body of the semicon-
20 ductor material in an oxidizing and/or steam
ambient, which also functions to grow a thick (5,000
to 10,000 Å) SiO$_2$ region 21 on the poly-silicon gate
as well as over the n+ source sites 22. The n+
sources are advantageously diffused to a depth of
25 approximately 1 micron as well as laterally, as
shown in Figure 7.

Next, the entire slice is etched in a suitable SiO$_2$
chemical etch, or by the use of a plasma etch, to
remove the originally deposited SiO$_2$ layer 14 which,
30 it will be recalled, is only approximately 2,000 Å
thick. Thus, the 5,000 to 10,000 Å SiO$_2$ region 21 will
not be substantially affected by this SiO$_2$ etch step.
Following the SiO$_2$ etch, some suitable Si$_3$N$_4$ che-
mical etchant, or some suitable plasma etch source,
35 is used to remove the original 2,000 Å deposited
Si$_3$N$_4$ layer 13. The structure as it appears at this
stage of the process is shown in Figure 8.

Next, the poly-silicon material in the gate region is
opened up using a third photo-lithographic step to
40 establish the pad areas. This third photo-lithographic
step is, again, non-critical and advantageously may
be used to etch the SiO$_2$ remaining in the region
where the pads will be formed.

Then, as shown in Figure 9, a layer of metalization
45 23 is evaporated or sputtered over the entire surface
of the wafer, e.g., to a depth of 20,000 Å. While
several metals may be used for this metalization
layer, Aluminum is the preferred material. Finally, in
the fourth photo-lithographic step, which is also
50 non-critical, the metal is etched to separate the gate
from the rest of the silicon surface, which of course
comprises the source electrode. With the above
described process, it is possible to achieve a center-
to-center gate spacing of 10 microns or less. Figure
55 10 is a view looking down on the top surface of the
wafer and illustrates quite clearly that the V-grooves
are etched in both the X and Y directions. In the
drawing, reference numeral 31 represents the gate
grooves, reference numeral 32 represents the source
60 grooves and rectangular areas 33 and 34 represent
the contact pads for the devices.

The structure shown in Figure 10 has, of course,
the classic "Manhattan" geometry and this may
pose a problem under some circumstances. The
65 problem is that although the sidewalls along each of

the four sides of each source area are the standard,
expected 111 crystal planes upon which the V-MOS
devices are formed, at each inside corner, where the
grooves intersect, faster etching 112 and 331 crystal
70 planes are exposed, resulting in undercutting. While
this undercutting may be minimized by manipulat-
ing the various etching compositions, e.g., by adding
small quantities of hydrazine to the etching solution,
as well as by manipulating the etching temperature,
75 or by the use of photomask compensation to assure
that rectangular corners are formed, these additional
steps complicate the manufacturing process and it
would be clearly advantageous if these additional
steps could be eliminated.
80 We have discovered that one way that this may be
done is to modify the topological layout of the
device, thereby eliminating corner undercutting en-
tirely, as well as providing the additional advantage
of increasing the active V-MOS groove periphery per
85 unit area, thereby giving still further increased
power and current density. The basis for this discov-
ery is the realization that the area at the intersection
of the V-grooves is "dead space" contributing
nothing to the active gate periphery and therefore
90 contributing nothing to the output current. Accord-
ing to the invention, the modified device incorpo-
rates at each intersection an additional source cell
area that is either coincident at the corners with the
existing cells or which slightly overlaps the existing
95 cells at each corner. This arrangement is shown in
Figure 11 and it will be evident that with such an
arrangement the etch will never "see" a convex
corner; thus, corner undercutting is eliminated. If
one compares the device shown in Figure 11 with
100 that shown in Figure 10, it is possible to compare the
active channel periphery for the repeat area of the
original design, which employed 5 micron wide
grooves and 5 micron × 5 micron source areas,
which yields a linear gate periphery of 20 microns
105 per 100 μM^2 area. The arrangement shown in Figure
11, on the other hand, yields for the same layout rule
a linear gate periphery of 32 microns with one
micron corner overlap and 40 micron gate periphery
for a coincident design. This represents a 60-100%
110 improvement in power density over the arrange-
ment shown in Figure 10 while at the same time
eliminating all the corner undercutting problems
previously mentioned.

Turning to Figure 11, consider the four source
115 regions 41, 42, 43, 44. In the modified device, the
region between the devices 46 that is not occupied
by the metalization 34 is configured as an additional
source region and, focusing on the cell area defined
by the dotted lines 47, it will be seen that, as
120 discussed, the additional source regions contribute
to the output current, as desired. Also, since the
additional source regions are in contact with the
corners of the main source region 42, the aforemen-
tioned undercutting will not take place, for the
125 reasons previously discussed.

In the arrangement shown in Figure 11, the gate
periphery per cell repeat area is 32 μM per 100 μM^2.
This contrasts with the figure of 30 μM per 100 μM^2
for the arrangement shown in Figure 10, which
130 represents a 6.67% increase in active current hand-

ling area. The arrangement shown in Figure 11 assumes a typical 1 micron center region overlap of the original source sites.

We will now discuss an alternate embodiment of
5 the invention which permits considerably fewer and far simpler processing steps, while at the same time keeping the number of photomasking operations to a minimum. The advantages of this alternate embodiment are (1) the source is self-registered to the
10 gate (e.g., to the groove masks); (2) only four photomasks are required including (a) the gate (groove) photomask, (b) the source contact photomask, (c) the gate pad contact photomask and (d) the metalization photomask. Of these, only the source
15 contact photomask requires any substantial degree of alignment tolerance; (3) the use of a shallow, n+ source diffusion with aluminum alloyed through the source to the body junction providing an excellent source to body short circuit, resulting in high
20 drain-to-source sustaining voltages which approach the drain-to-body junction breakdown voltages.

As shown in Figure 12, the starting point for the alternate embodiment is the same as shown in Figure 1 for the first embodiment; that is, an n+
25 doped silicon substrate 10 having double layer eiptaxial films 11 and 12 grown thereon. For the second embodiment of the invention, the p− layer 12 is approximately 2.75 microns thick and has a resistivity of 0.5 ohm-centimeters. As before, the
30 thickness of the n− layer 11 is a function of the voltage that the device is to withstand. For example, for a 100 volt device, the n− layer 11 would typically be 1.6 ohm-centimeters in resistivity and approximately 10 microns thick. The substrate typically
35 comprises an Sb-doped, 100 crystal orientation, silicon substrate having a resistivity of from 0.005 to 0.01 ohm-centimeters.

The first step in the manufacture of the alternate embodiment is to diffuse an n+ dopant over the
40 entire top surface of the water, advantageously using a compound such as arsenic to achieve shallow X(j). This is depicted by layer 51 in Figure 12. Next, as shown in Figure 13, a layer of silicon nitride is deposited over the n+ layer 51 using either a high
45 temperature deposition technique or a low temperature LPCVD process. The Si_3N_4 4 layer is represented by reference numeral 52 in Figure 13. Next, a layer of SiO_2 is put down on top of the Si_3N_4 using any conventional deposition technique. This layer is
50 designated as layer 53 in Figure 13.

As shown in Figures 14 and 15, the next step in the process is to open apertures 55 in the silicon dioxide layer 53 at the precise location that the V-shaped grooves are to be formed. In a manner analogous to
55 that previously discussed with respect to Figures 3 and 4, the underlying exposed silicon nitride and other layers are then etched, using any suitable etching process. For example, a standard ethylenediamine pyrocatectol pyrazin solution. The wafer is
60 then thoroughly cleaned.

Next, gate oxide material is grown in the V region, as indicated by reference numeral 56 in Figure 15. This material, typically SiO_2, is then annealed. Next, a layer 57 of poly-silicon is deposited over the entire
65 surface of the wafer to a thickness of from 5,000 to

10,000 Å. Then, phophorous is diffused into the poly-silicon to bring the sheet resistance of the material down to as low a value as possible, ideally in the range of 15 ohm/square. Advantageously, the
70 poly-silicon is firmly oxidized during the diffusion process to a depth of about 3,000 to 5,000 Å.

Next, a second photo-lithographic step is used to open up the contact regions between the V-grooves. The alignment tolerance for this step is again
75 non-critical, since this opening can occur anywhere within the 5 micron spacing between adjacent V-grooves. Next, the SiO_2 layer is etched using, for example, a buffered HF solution, and the poly-silicon is then etched down to the nitride layer using, for
80 example, an EDPP slow-etch process. The photoresist is then stripped and cleaned and the sidewalls of the exposed poly-silicon firmly reoxidized. Finally, the nitride is etched out of the contact areas to yield the configuration shown in Figure 16, where refer-
85 ence numeral 58 represents the reoxidized sidewalls of poly-silicon layer 57. Then, a third photolithographic step is used to open up the gate bonding pad exposing doped poly-silicon. After this is done, the wafer is metalized with aluminum or a
90 silicon flashed aluminum (1 - 2%) alloy at a sufficiently high temperature, e.g., 500 - 575°C such that the alloying goes through the thin n+ source diffusion 51 and forms a short circuit between the p− substrate 12 and the n+ source junction layer 51.
95 This is a very critical step, as it is necessary to achieve a sustaining breakdown voltage BVDS of at least 80% of the junction breakdown voltage in the n− to p− junction. Finally, using a fourth and last photo-lithographic step, the top surface of the wafer
100 is coated with aluminum which is then patterned to form the gate bonding pads and the source pads which comprise the remainder of the upper surface of the devices. There is an alternate process which may be used, if desired, to form the gate contacts. In
105 this embodiment, after the polysilicon is subjected to the phophorous doping step, a 1,000 Å thick layer of silicon nitride is deposited over the entire surface of the wafer. Then, using a second photo-lithographic step, the nitride is removed from the entire surface
110 of the device, except where the gate bonding area is to be. Then, the poly-silicon is etched down to the nitride layer, as in the second embodiment of the invention and the sidewalls thus exposed are reoxidized. Finally, metalization is effected through the
115 source n+ region, as before, and the metal patterns required for the gate bonding pads and source pads are photo-delineated.

A person skilled in the art can make various changes and substitution to the layout of parts
120 shown without departing from the spirit and scope of the invention.

CLAIMS

125   1.   A V-MOS, field-effect, semi-conductor device having gate, source and drain electrodes, which comprises: a planar, doped, silicon substrate; a first, doped, silicon layer, epitaxially grown on said silicon substrate; a second, doped, silicon layer epitaxially
130 grown on said first silicon layer; characterized by a

plurality of spaced-apart, parallel, first V-grooves extending through said first and second layers; a plurality of spaced-apart, parallel, second V-grooves extending through said first and second layers but

5 not into said substrate, said first and second V-grooves having doped poly-silicon on the walls thereof, being orthogonally oriented with respect to one another, and defining by their intersections at least one generally rectangular, isolated, electrically-

10 floating region of the second doped layer which acts as the body electrode of the device, the remaining non-isolated regions of said second layer acting as the gate electrode of the device, said substrate acting as the drain electrode.

15   2. A semi-conductor device according to claim 1, wherein said first V-grooves extend through said first and second layers but not into said substrate.

  3. A semi-conductor device according to claim 1 or 2, further characterized by a heavily doped n^+ or

20 p^+ region on the surface of said second epitaxial layer.

  4. A semi-conductor device according to claim 1, wherein said first V-grooves extend through said first and second layers into said substrate; a plurality

25 of other regions of said second doped layer, said regions acting as an additional source region, each region electrically contacting at least one corner of the four immediately adjacent, electrically-floating one regions, an individual device being defined by

30 (a) one electrically floating source region and portions of the four immediately adjacent additional souce regions; (b) the V-groove gate electrode; and (c) the substrate which acts as the drain electrode for the device.

35   5. A semi-conductor device according to any one of claims 1-4, wherein said substrate comprises 100, single crystal silicon, heavily doped n^+, said first epitaxial layer comprises lightly doped n^- silicon, and said second layer comprises lightly doped p^-

40 silicon.

  6. A semi-conductor device according to any one of claims 1-4, wherein said substrate comprises 100 single-crystal silicon, heavily doped p^+, said first epitaxial layer comprises lightly doped n^+ silicon,

45 and said second epitaxial layer comprises lightly doped p^- silicon.

  7. A semi-conductor device according to claim 5 or claim 6 wherein the regions in said second silicon layer immediately adjacent to the walls of said

50 V-grooves are doped n^+ thereby to form source regions adjacent to said grooves.

  8. A method of manufacturing a V-MOS, field-effect, semi-conductor device having gate, source, and drain electrodes, which comprises the steps of:

55 forming first and second, oppositely-doped, epitaxial layers on a planar, doped, silicon substrate; opening along a first direction, at least two, spaced-apart, parallel, first V-grooves in said first and second layers, said grooves extending downwardly

60 but not into said substrate; opening along a second direction orthogonal to said first direction, at least two, spaced-apart, parallel, second V-grooves extending downwardly and defining by their intersections at least one, generally rectangular, isolated,

65 electrically-floating region of the second doped layer

which acts as the source electrode of the device; depositing a layer of poly-silicon on the walls of said grooves; and then, doping said poly-silicon layer thereby to form the gate electrode of said device.

70   9. A method according to claim 8 further characterized by forming a plurality of second regions in said second, doped, epitaxial layer, said regions acting as additional source regions, each region electrically contacting at least one corner of the four

75 immediately adjacent electrically-floating first regions, an individual device being defined by (a) one electrically-floating source region, and portions of the four immediately adjacent additional regions; (b) the V-groove gate electrode; and (c) the substrate

80 which acts as the drain electrode of the device.

  10. A method according to claim 8 or 9, wherein said doping step comprises: doping regions in said second epitaxial layer which are immediately adjacent to the walls of said grooves, thereby to form

85 source regions adjacent to said grooves.

  11. V-MOS field effect semiconductor devices substantially as hereinbefore described with reference to the accompanying drawings.

  12. Methods of manufacturing V-MOS field effect

90 semiconductor devices substantially as hereinbefore described with reference to the accompanying drawings.

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